

The EDRA project: Bringing Efficient Reconfigurable Architectures to the Amazon Cloud for Bioinformatics Applications

FPL 2020: Research Projects Event

Speaker: Dimitris Theodoropoulos dtheodoropoulos@isc.tuc.gr

Nikolaos Alachiotis nalachiotis@isc.tuc.gr

Demo: Andreas Brokalakis abrokalakis@mhl.tuc.gr

Dionisios Pnevmatikatos pnevmati@ece.tuc.gr



Telecommunication Systems Institute

Technical University of Crete

Campus – Akrotiri

73100 Chania, Crete, Greece

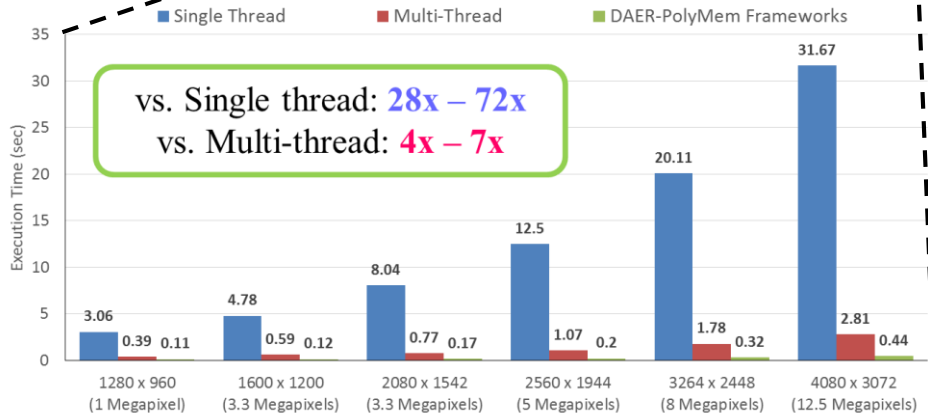
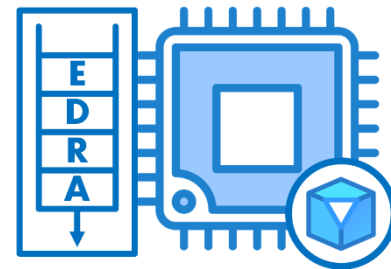


The EDRA concept

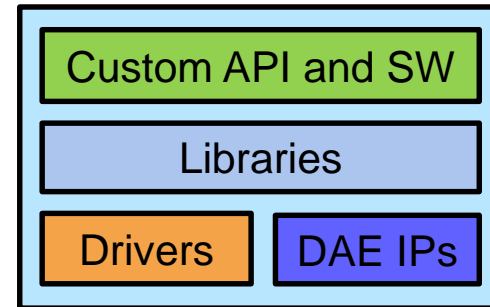
Exploiting eXascale Technology with Reconfigurable Architectures



Decoupled Access-Execution Reconfigurable (DAER) framework



EDRA machine image
aws

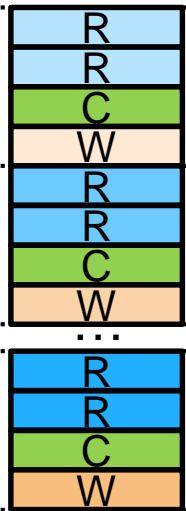




The EDRA concept

- **EXTRA FET-HPC* Decoupled Access – Execute Reconfigurable (DAER) framework**

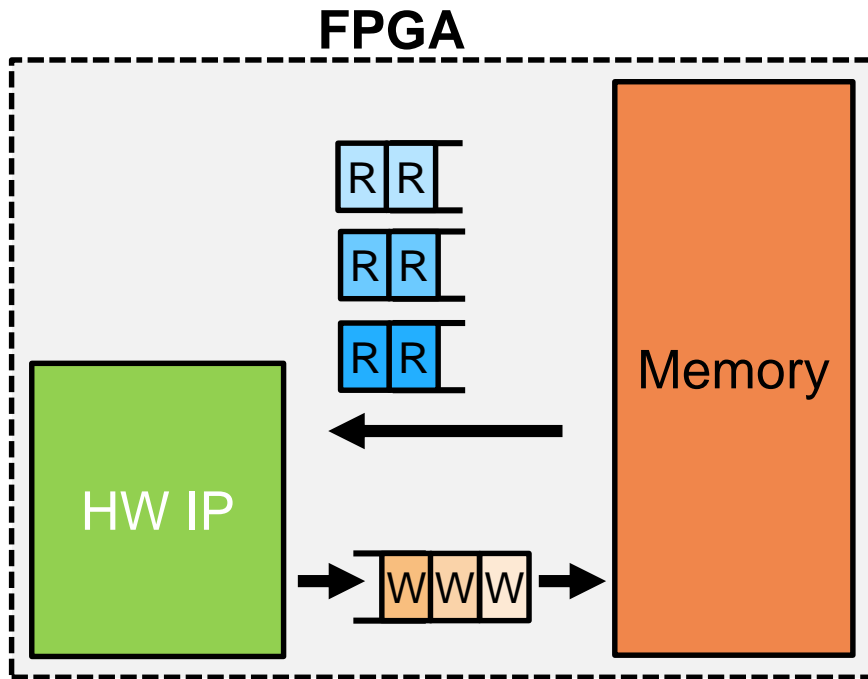
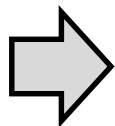
for-loop flow



$$C[0]=A[0]+B[0]$$

$$C[1]=A[1]+B[1]$$

$$C[N-1]=A[N-1]+B[N-1]$$



* <https://www.extrahpc.eu/>





The EDRA concept

■ EDRA: EXTRA DAE Reconfigurable Architecture

■ Objectives

1. Automate software workflow for DAER-compatible accelerators
2. Integrate the EDRA framework with the AWS FGPA infrastructure
3. Publish an EDRA Amazon Machine Image (AMI)

Invest on the DAER architecture
as an FPGA cloud service



■ First MVP

- Publish on the AWS marketplace a VM for accelerating phylogenetics analysis





Demo application

- **RAxML** (Randomized Axelerated Maximum Likelihood) is a widely employed phylogenetic inference software
- Dominant kernel
 - *Phylogenetic Likelihood Function (PLF)* → from **50% to 80%**
 - Hardware kernel implemented on AWS F1 instances
 - The kernel architecture is based on the Decoupled Access Execute design paradigm
 - Xilinx SDAccel framework + HLS to describe the accelerator and OpenCL/Xilinx XRT integration with RAxML

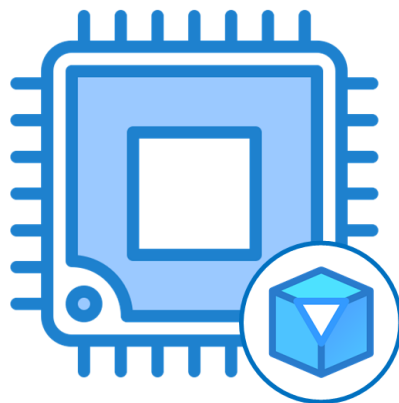




Demo application

- **Communication with host CPU**
 - Two 512-bit interfaces to stream input data to the execution pipeline
 - One 512-bit interface streams the results back to memory
 - One 64-bit memory interface reads kernel configuration parameters
 - Double buffering
- **Hardware specifications**
 - Initiation interval at 2 cc
 - Design frequency at 222MHz
- **Performance**
 - Up to 6x compared to the original software-optimized RAxML version





Thank you



edrah2020@isc.tuc.gr



<https://edra-project.eu/>



@ProjectEdra



<https://www.linkedin.com/groups/8790812/>

